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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/699,135	10/31/2003	Ulf Tohsche	W&B-INF-1980	3466

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EXAMINER	
NGUYEN, HIEP	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 06/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/699,135	TOHSCHE, ULF	
	Examiner	Art Unit	
	Hiep Nguyen	2816	

-- Th MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *31102003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Abstract

Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to **a single paragraph** on a separate sheet within the range of **50 to 150 words**.

Specification

The disclosure is objected to because of the following informalities: the disclosure "the first switching element 8... the first inverter circuit 6" on lines 14-20 of page 13 is not relevant. Regarding to figure 1 of the present application, transistors (T1) and (T2) must be turned on to provide "programming potential" to nodes (K1) and (K2). According to page 17, lines 12-17, when the clock is **high, no data is forwarded** to the first and second switching elements (8) and (9). Thus, when transistors (T1) and (T3) of the switch elements is turned on with the **high level** of the clock signal **no data can pass through the circuit** for providing "a programming potential" to nodes (K1) and (K2). It is also not clear how the "programming potential" can be generated and applied to the first and second nodes (K1) and (K2). The Applicant is requested to explain what is the "programming potential" and how it can be generated. According to the connection of the switching elements (8) and (9), no high potential level can be generated by the switching elements (8) and (9).

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1, 9, 10 and 16 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not

described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

In claim 1, the recitation "said data acceptance unit being **adapted to** allocate, dependent upon the data signal present and the **clock signal** present, **predetermined programming potential** either to said first input or to said second input and to apply **no potential** to the respective other input of said first and second inverter circuits..." is non enable because in order to have data (D) transfered to the storage unit, inverters (10) and (11) must be enabled by a low clock (CLK). But when the clock is low, transistors (T1) and (T3) of switching elements (8) and (9) are turned off. Thus, data D) or a voltage derived fron data (D) cannot be forwarded to the storage unit (4). It is also unclear what the "no potential" and the "predetermined potential" are meant by. The same analysis is true for claim 16.

Claims 9 and 10 are non-enable because according to figure 1, clock (CLK) needs to be at **low** potential level in order to **forward data** (D) to the switching elements (8) and (9). With the low level of the clock signal, switching elements (8) and (9) are inhibited thus, no data can be stored in the storing device.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction and /or clarification is required.

Regarding claims 1 and 16, the recitation "and said data acceptance unit being **adapted to** allocate, dependent upon the data signal present and the clock signal present, a predetermined programming potential either to said first input or to said second input and to apply **no potential** to the respective other input of said first and second inverter circuits" is indefinite because it is unclear as to how the acceptance circuit must be **adapted** to provide the "predetermined programming potential". See In re Rohrbacher 128 USPQ 117. Figure 1 of the present application and the specification (spec. page 17, lines 7-12) show that the data can only forward to the switching elements (8) and (9) when the clock is at **low** potential level.

But when the clock is at **low** potential level, the n-type transistors (T1) and (T3) of the switching circuits are turned off and the switching elements (8) and (9) are disabled. Thus, no data is sent to the storage unit when the clock (CLK) is at **low** level. It is also not clear what the "**no potential**" is meant by. The same analysis is true for claim 16.

Regarding claims 2-11, the recitations "first switching element", "second switching element", "first level", "second level" of the clock signal", "first level", "second level" of the data signal", the "first and second partially clocked inverters" are confusing. The Applicant is requested to show on the drawing these elements and to show what are the first and second levels (low/high) of the clock and data signal.

Regarding claims 5 and 6, the recitation "the **second level** of the clock signal **and** the **first level** of the clock signal **given** (?) **a presence** of the second level of the data signal and to apply no potential to said first switching element **given** (?)a presence of the first level of the clock signal and the first level of the data signal" is indefinite because it is not clear what it is meant by. As understood by the examiner, the data (D) is inverted by circuit (T5-T7) and is transmitted to the first switching element (8) when the clock (CLK) is at the second level (low). When the clock is at the first level (high), data is not transmitted. It is not clear what the "no potential" is meant by. It is not clear what the recitation "...given a presence..." in the claim is meant by. Explanation is required.

Regarding claims 7 and 8, the recitation "said second partially clocked inverter is connected to said output of said first partially clocked inverter to apply a **non-inverted data signal** to said **second** switching element in the event the **second level** of the clock signal and to apply **no altered potential** to said second switching element in the event of the **first level** (?) of the clock signal" is indefinite because it is confusing. It is not clear what is the difference between the "a **non-inverted data signal**" and the "**no altered potential**". Figure 1 of the present application shows that when the clock signal is at low level (second level), data (D) is transmitted to the second switching element (9) without being altered. In the event of the first level of the clock signal (high), the first and second partially clocked inverters are disabled and no data is transmitted to the second switching element (8) .The same analysis is true for claim 8. To clarify the indefiniteness if the claim, the Applicant is request to point out in the drawing the following limitations: the first and second partially clocked inverters, the

first and second switching elements, the non-inverted data, the no altered potential and to define what is the first level of the clock signal (high or low), the second level of the clock signal. Note that the **first level** of the clock signal (high or low), the **second level** of the clock signal (high or low) should be **homogeneous for all the claims**. The Applicant is also requested to shows what is the **difference** between the "non-inverting data" and the "no altered potential" of the data.

Regarding claim 9, the recitation " wherein said first and second partially clocked inverters are configured, in an event of a change in the clock signal from the **second level** to the **first level** the clock signal from **given** (?) an unchanged data signal, to present the inverted data signal at said output of said first partially clocked inverter and to present the non-inverted data signal at said output said second partially clocked inverter until the data signal is stored in said storage unit" is indefinite because it is misdescriptive. Figure 1 of the present application and the specification (page 17, lines 7-12) show that the data can only forward to the switching elements (8) and (9) when the clock is at the second level (low potential level). When the clock is at the first level (high), no data is transferred. It is not clear what "from **given** (?) an unchanged data signal" is meant by. The Applicant is requested to define what are the first and second levels of the clock signal (high or low). Note that the **first level** of the clock signal (high or low), the **second level** of the clock signal should be **homogeneous for all the claims**. The same analysis is true for claim 10.

Regarding claim 12, the recitation "in an event of a **first level** of the clock signal, to apply either: the inverted data signal to said first switching element if a second level of the data signal is present; or **no potential** to said first switching element if a first level of the data signal is present" on lines 13-19 is indefinite because it is misdescriptive. The **first level** of the clock signal is a **high level** and a high level of the clock disables the first and second "clocked gate" thus, **no data is transmitted**. It is not clear what "**no potential** to said first switching element if a first level of the data signal is present" is meant by. As understood by the examiner, when the clock signal is at the second level (low) the low or high potential of the input data (D) is transmitted to the first switching element (8). The Applicant is requested to explain what the "no potential" is meant by. The recitation " to apply a ground potential to said first switching element in an event of a **deactivation signal**" is indefinite because it is

misdescriptive. Figure 2 of the present application shows that the "deactivation signal" **itself** cannot apply a ground potential to the first switching element as recited. The recitation "a first partially clocked **gate**" (or a second partially clocked gate) is indefinite because it is unclear as to this "a first partially clocked gate" is the same or different than the "a first partially clocked **inverter**" in claim 5. The Applicant is requested to point out these elements in the drawing.

Regarding claim 13, the recitation "to apply **a ground potential** to said second switching element **at least one** of **in** (?) an event of the **first level** of the clock signal and in an event of a deactivated activation signal" is indefinite because it is misdescriptive. Assume that if the **second level** of the clock signal is **low** then the first level of the clock signal is **high.** When the clock is **high**, transistors (T7) and (T9) are turned **off** and no data (ground potential) is forwarded to the second switching element (9).

Regarding claims 14 and 15, the recitation "... in the event of the first level of the clock signal **dependent upon the data signal stored in said storage unit**" is indefinite because it is not clear how the **first level of the clock signal** can be **dependent upon** the data signal stored in said storage unit. Explanation is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Kojima et al. (US Pat. 6,445,217).

Regarding claims 1 and 16, figure 6 and 8 of Kojima show a flip-flop, comprising:

a clock input (C), a data input (D), a non-inverted output (Q), an inverted output (Q/);

a data acceptance unit (128, 129, 630, 632) having a first second switching element (630, 632);

a storage unit (134-137) having first and second inverter circuits (134, 135) connected in a feedback loop to provide feedback between said first and second inverter circuits;

Depending upon the data and the clock signal, the switching elements (630, 632) apply a "predetermined programming potential " and a ground potential to the inputs of the storage unit (134-137).

Claims 1-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Oklobdzija et al. (US Pat. 6,232,810).

Regarding claims 1 and 16, figure 6A and 7 of Oklobdzija show a flip-flop, comprising:

a clock input (Clk), a data input (D), a non-inverted output (Q), an inverted output (Q/);

a data acceptance unit (101, 34, 36) having a first second switching element (T1, 34 and T5, 36);

a storage unit (32) having first and second inverter circuits (82, 84) connected in a feedback loop to provide feedback between said first and second inverter circuits;

Depending upon the data and the clock signal, the switching elements apply a "predetermined programming potential" and a ground potential to the inputs of the storage unit (32).

Regarding claims 2-4, figures 6A and 7 show that the first switching element (T1, 32) is activated when the clock is high and the data is at high level and is inhibited when the clock is at low level.

a. Regarding claims 5 and 6, the "a first partially clocked inverter" comprising transistors (T2-T4) that convert a high level data input to a low level signal (S/). The first switching element (T1, 34) receives low-level signal (S/) when the clock signal is high and the data is high. Signal (S/) becomes low when the clock is high and the data is low.

Regarding claims 7-9, figures 6A and 7 show that the second switching element (T5, 36) is activated when the clock is high and the data is at high level and is inhibited when the clock is at low level.

Regarding claim 10, figure 7 shows that when the clock changes from a low level to a high level, data (D) is transferred to storage unit in complementary form (S/, R/) and to be stored.

Claims 1 and 11-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Yee et al. (US Pat. 6,720,813).

Regarding claims 1 and 11, figure 3 of Yee shows a flip-flop, comprising:

a clock input (Clk), a data input (d), a non-inverted output (q), an inverted output (d-inv);

a data acceptance unit (26) having a first second switching element (64, 66);

an activation input (ena) for activating the flip-flop.

a storage unit (30) having first and second inverter circuits connected in a feedback loop to provide feedback between said first and second inverter circuits;

Depending upon the data and the clock signal, the switching elements apply a "predetermined programming potential " and a ground potential to the inputs of the storage unit (30). When the activation input signal (ena) is low, transistors (64) and (66) are turned on and data (d) and (d-inv) are transferred to the storage unit (30) (col.4, lines 21-36).

Regarding claims 12-15, the " first partially clocked gate" is element (40) and the first switching element is transistor (64). When (ena) signal is high and data (d) is high, transistor (112) is turned on and a low level potential is applied to the first switching element (64). The data is then stored in the storage unit (30).

Claims 1-10 and 16 are rejected under 35 U.S.C. 102(b) as being anticipated Japanese reference No. 10093397.

Because of the confusion of the language of the claims, assume that the first switching element is element (6,7), the second switching element is element (4, 5), the first level of the clock signal and the data signal is a high level and the second level of the clock

signal and the data signal is a low level, the first partially clocked inverter is (B), the second partially clocked inverter is (A).

Regarding claims 1 and 16, the reference shows a flip-flop, comprising:

a clock input (CLK), a data input (D), a non-inverted output (Q), an inverted output (QN);

a data acceptance unit (A, B, 4, 5, 6, 7)) having a first second switching element (4, 5 and 6, 7);

a storage unit (8, 9) having first and second inverter circuits connected in a feedback loop to provide feedback between said first and second inverter circuits;

Depending upon the data and the clock signal, the switching elements apply a "predetermined programming potential " and a ground potential to the inputs of the storage unit.

Regarding claim 2, when the data signal (D) and the clock signal (CKL) are at high level, the first switching unit (6, 7) in activated and when the data signal or the clock signal is at low level, the first switching unit is inhibited.

Regarding claims 3 and 4, when the clock signal (CKL) are at high level and the data signal (D) is at low level, the second switching unit (4, 5) in activated and when the clock signal is at low level and the data signal is at high level, the first switching unit is inhibited.

Regarding claims 5 and 6, the first partially clock inverter (B) has an output coupled to the first switching element (6, 7). When the clock signal is at low level (second level) and the data is at low level (second level), a low level signal is applied to first switching element (6, 7).

Regarding claims 7 and 8, the second partially clocked inverter (A) is coupled to the second switching element (4, 5). The second partially clocked inverter (A) applies an inverted data signal (DN) to the second switching element (4, 5) when the clock signal is low. The first partially clocked inverter (B) applies an non-inverted data signal (D) to the first switching element (6, 7) when the clock signal is low.

Regarding claim 9 and 10, the circuit of the Japanese reference clearly shows the transferring of data depending upon the level of the data and the clock signals. When the

clock signal changes from a low level to a high level, data (D) is transferred to storage unit in complementary form (D and DN) and to be stored in the storage unit.

Conclusion

The claims have serious 112, first and second paragraph problems. The Applicant is requested to amend the claims so that one skilled in the art can understand the meaning of the claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep Nguyen whose telephone number is (571) 272-1752. The examiner can normally be reached on Monday to Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hiep Nguyen
06-09-04

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PRIMARY EXAMINER